LLC Converter with Auxiliary Switch for Hold Up Mode Operation

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***Abstract*— This paper proposes a new half bridge (HB) LLC resonant converter with pulse width modulated (PWM) auxiliary switch (sLLC converter) for hold-up mode operation. The proposed sLLC converter works with synchronous rectifier (SR), which is suitable for low output voltage applications. The magnetizing inductor can be designed with large value to reduce the circulation loss. In the proposed sLLC converter, the auxiliary switch and diode branch will provide charging path for the resonant inductor. For nominal 400V input, sLLC achieves same performance as conventional LLC converter, and all the good features such as soft switching are naturally retained. For slight input voltage fluctuation, frequency modulation is used to regulate the output voltage. When the input voltage drops further, HB switches will operate at constant minimum frequency, and the auxiliary switch will operate in PWM mode to energize the resonant inductor with 400V bus directly during hold up period, thus the output voltage can be maintained at desired level. To verify the effectiveness of the proposed sLLC converter, operational principle and equivalent circuit will be carefully explained and analyzed in this paper. A 300W prototype is built for 250V-400V input, 12V output application.**

Keywords*— LLC; hold up; high voltage gain; auxiliary switch; PWM; telecom power supply

I. INTRODUCTION

Recently, considerable research has been conducted on LLC-based telecommunication power supplies. PFC stage converts the AC line into 400V DC, which is further converted by the DC/DC stage to 12V DC. The typical structure is shown in Fig. 1. LLC resonant converter is widely used as the DC/DC stage because it achieves high efficiency as well as low EMI performance due to the inherent zero voltage switching (ZVS) on the primary MOSFETs and zero current switching (ZCS) on the secondary rectifiers.

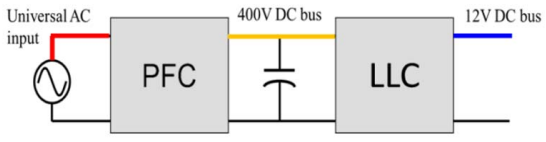

Fig. 1. Structure of the front end converter

A critical issue for telecom power supply is the hold up problem illustrated in Fig. 2. When the AC line fails, the 400V bus voltage drops continuously. It is desired the 12V DC be maintained for several tens of milliseconds, until the UPS takes over [1]. Conventional LLC is not suitable for hold up operation. If an LLC converter is designed to achieve high voltage gain, the efficiency at nominal 400V input will be severely penalized [2], [3]. Therefore, to solve the hold-up problem, the primary objective is:

1) to increase the operational input voltage range of the LLC converter;
2) to maintain high efficiency for the nominal 400V input operation.

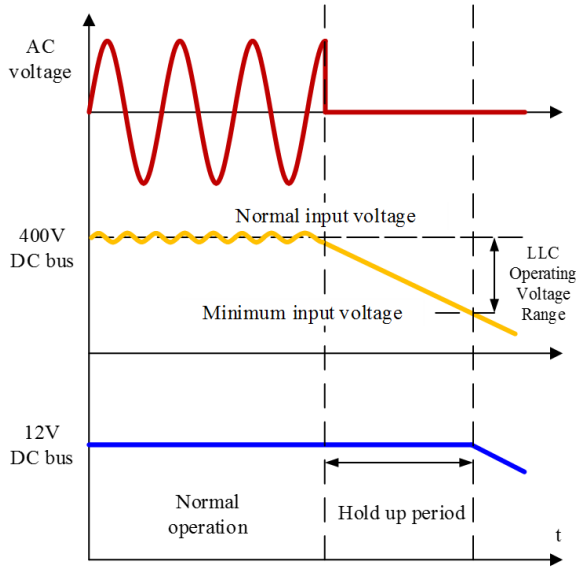

Fig. 2. Hold-up problem process

To achieve high efficiency at 400V operation, the transformer turns ratio needs to be properly designed to ensure that the converter operates at resonant frequency at 400V input. Moreover, the magnetizing inductance should be optimized to reduce the circulating current in the resonant tank as much as

possible while maintain ZVS for the HB FETs. At last, for 12V output applications, on the secondary side, synchronous rectifiers (SR) should be used instead of diode rectifiers, as the forward voltage drop of diodes would be a deal breaker of the whole efficiency.

To improve the LLC converter's operational voltage range to meet hold-up time requirement, quite a few methods have been proposed.

Among them, the most straightforward way is to employ a cascaded structure with a baby boost converter [4]. However, the additional power diode will reduce the efficiency at nominal 400V operation. Besides, the two stage configuration is complicated, and consequently costly.

A category of approaches solving the hold-up problem by utilizing auxiliary windings on the secondary side of the main transformer [5], [6]. Generally speaking, as long as the LLC converter reaches the peak gain, the switch-controlled auxiliary windings will take over the secondary side power transfer. Increased transformer turns-ratio helps to achieve higher voltage gain of the LLC converter during the hold-up period. Also, the discrete design between nominal 400V operation and hold-up state operation can maintain high efficiency for 400V input. However, usually the main transformer is the most bulky and lossy part of the converter, thus adding extra windings makes it even more difficult to optimize the transformer from both efficiency and power density improvement point of view.

By driving the half-bridge MOSFETs with asymmetric pulse-width modulation (APWM) rather than conventional frequency modulation (FM), LLC converter can improve output-to-input voltage gain without any additional components [7]. This method, however, suffers from limited peak gain enhancement. Besides, once the resonant tank is designed, the maximum gain that APWM control could achieve is also determined, which is not practical in terms of design flexibility.

A critical insight was revealed in [8] that if the resonant tank can be charged with more energy during one switching cycle, LLC converter achieves higher gain. To charge the resonant tank more, the secondary windings are short circuit for a certain period of time in every switching cycle. The downside of this method is that quite a few components need to be added in the power train on the secondary side, which causes size increasing and efficiency reducing.

Based on [8], a few improving methods propose to adopt either Boost PWM discontinuous current mode (DCM) control [9] or phase shift control on LLC topology[10], [11]. The common principle of these methods is that, in each switching cycle, the resonant tank will be short circuit on either primary side or secondary side by auxiliary switches for a period of time, so that the resonant inductor can be energized more quickly, hence store and transfer more power. The nominal 400V efficiency remains uninfluenced as compared to a conventional LLC optimized for 400V input voltage. However, for [9], [10] and [11], none of the method is compatible with SR, thus cannot be used in low output voltage applications.

In this paper, sLLC converter is proposed to solve the hold-up problem while avoiding the aforementioned issues. The proposed sLLC converter works with SR, thus it is particularly suitable for low output voltage applications in telecommunication field. The design for hold up operation is independent of nominal 400V operation design, in which the magnetizing inductor can be designed with large value to reduce the circulation loss, such that the converter achieves optimal efficiency at nominal 400V. During hold up period, the auxiliary switch operates in PWM mode. When the auxiliary switch is turned ON, the input DC bus voltage, rather than the capacitor voltage in conventional LLC converter, is constantly applied to the resonant inductor, thus the resonant inductor accumulates more energy in shorter time, and high voltage gain is achieved. This paper is organized as follows: Section II presents the operating principle and mode analysis; Section III gives the detailed circuit analysis; Section IV demonstrates the experimental results; and Section V concludes the paper.

II. Operation Principle Of The Proposed Converter

Fig. 3 shows the proposed LLC converter with auxiliary switch (sLLC) for hold-up operation. The resonant tank is connected to 400V bus and middle point of the half bridge respectively. The magnetizing inductor could be integrated into the main transformer, while the resonant inductor L_r and resonant capacitor C_r are external. The charging branch consisted of one diode D_a and one MOSFET Q_a connects the resonant inductor L_r and the primary ground. C_a is the capacitor paralleled to Q_a. It should be noted that the Q_a is ground referenced, which enables simple driving.

When the input voltage is around nominal 400V, the auxiliary switch is kept OFF. The sLLC converter operates just

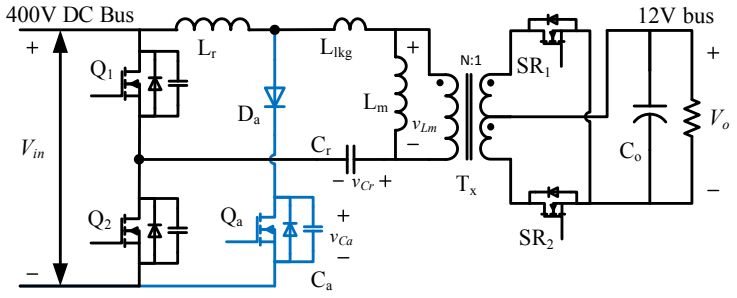

Fig. 3. Proposed sLLC topology with SR

like the conventional half bridge LLC converter. Thus, all the desirable features of LLC converters are automatically retained. Besides, the parameter design of the resonant components (L_r, C_r, L_m) only considers nominal 400V efficiency, which means that magnetizing inductor could be relatively large value to reduce the circulating magnetizing current, and to improve the efficiency. Frequency modulation (FM) is still used to regulate the output voltage when the input voltage drops slightly (i.e. switching frequency reduces with input voltage reducing). This is good to address the low frequency fluctuation on 400V bus from the PFC stage.

If the input voltage reduces to a level that the LLC converter cannot maintain the required output voltage level, the auxiliary switch will start to operate. During the positive half cycle when Q_2 is ON (source injects energy to the resonant tank), the auxiliary switch turns ON for certain period of time of a switching period, allowing the resonant inductor to be charged directly by the bus. It is more effective to boost the stored energy in the resonant inductor with the 400V bus than the resonant capacitor (the case in conventional LLC converter), thus sLLC transfers more energy in one switching cycle to achieve higher DC gain. The longer the auxiliary switch is ON, the more energy will be stored, and the higher gain can be achieved. During the hold-up period, Q_a will control the charging time of L_r to regulate the output voltage. C_a is used to absorb the voltage spike from the leakage inductor L_{lkg} when turning off Q_a. D_a provides unidirectional charging path, preventing C_a and the parasitic capacitor of Q_a from resonating during the normal operation. The key waveforms of the proposed sLLC converter during hold up period is shown in Fig. 4, in which G_{Q1}, G_{Q2} and G_{Qa} are the gate signals; i_{Lr} and i_{Lm} are the resonant inductor current and the magnetizing current in the primary side; v_{Cr} is the voltage stress on resonant capacitor; v_{Lm} is the voltage across the magnetizing inductor; i_{Da}, i_{Qa} and i_{Ca} are the current stresses in the auxiliary diode, auxiliary switch and paralleled capacitor; v_{Ca} is the voltage stress across Q_a and C_a; i_{SR1} and i_{SR2} are the secondary current; and I_o is average load current.

During hold up period, the operation in each switching cycle can be divided into 8 modes (M1~M8). The equivalent circuits are shown in Fig.5.

Mode 1 (M1): Q_2 and Q_a are turned ON at t_0. L_r will be charged by the bus voltage, so that i_{Lr} increases linearly and sharply. L_{lkg}, L_m and C_r will short circuit and resonate. The magnetizing current is negative during M1. No current will go through the transformer, and the output capacitor C_o discharges.

Mode 2 (M2): Q_a turns OFF at t_1 while Q_2 remains ON. L_r current will be released through the transformer. SR2 will conduct to charge C_o. Sudden change of current path will cause voltage spike on L_{lkg}, which will be absorbed by C_a. The capacitor voltage reaches its maximum at t_2. Large C_a and small L_{lkg} will reduce the voltage spike.

Mode 3 (M3): L_r, L_{lkg}, and C_r will resonate in M3 with Q_2 ON. SR2 conducts to charge C_o. The transformer will be clamped by the output voltage V_o, thus magnetizing inductor current i_{Lm} increase linearly. At t_3, i_{Lr} meets i_{Lm}, and the SR current drops to zero.

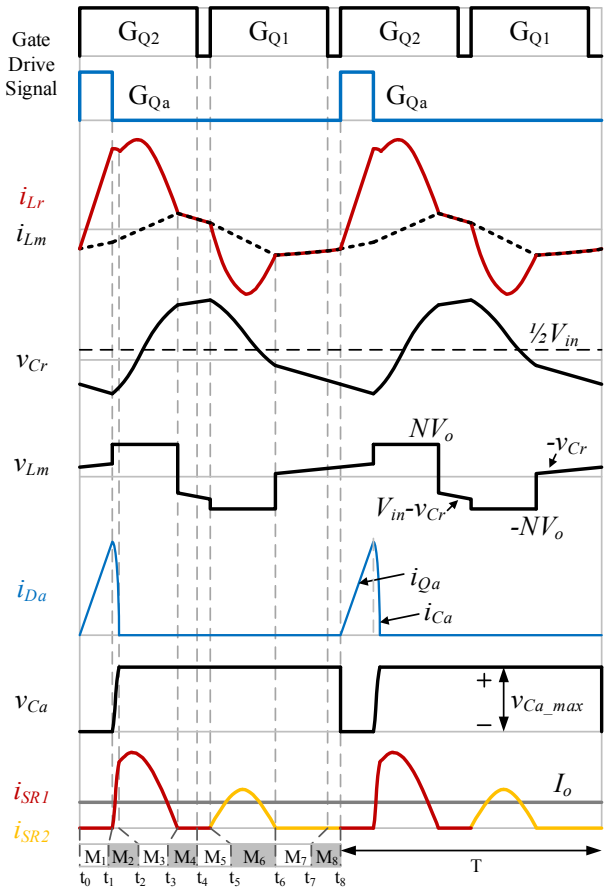

Fig. 4. Key waveforms of sLLC during holdup period

Mode 4 (M4): In M4, L_m will resonate together with L_r, L_{lkg}, and C_r. Transformer is in idle mode while the load current is provided by C_o. At t_4, Q_2 is turned OFF.

Mode 5 (M5): Both Q_1 and Q_2 are OFF during M5, the dead time. The resonant current will charge the parasitic capacitor of Q_2 while discharge that of Q_1. When the voltage across Q_1 drops to zero or so, the body diode of Q_1 conducts, clamping the voltage of Q_1 at around zero volts, thus, ZVS is achieved for Q_1 when it is turned on at t_5.

Mode 6 (M6): L_r, L_{lkg}, and C_r will resonate in M6 with Q_1 ON. SR1 conducts to charge C_o and powering the load. The transformer will be reversely clamped by the output voltage V_o, thus magnetizing inductor current i_{Lm} decrease linearly. At t_6, i_{Lr} meets i_{Lm}, and i_{SR1} drops to zero.

Mode 7 (M7): L_m will resonate jointly with L_r, L_{lkg}, and C_r in M7. Transformer power transfer is cutoff while the load current is provided by C_o. At t_7, Q_1 is turned OFF.

Mode 8 (M8): M8 is the dead time that the HB switches are OFF. The parasitic capacitor of Q_1 will be charged and that of Q_2 discharged by the resonant current. ZVS is achieved for Q_2 when it is turned on at t_8.

After M8, Q_2 and Q_a will be turned ON, and the converter operates in M1 again.

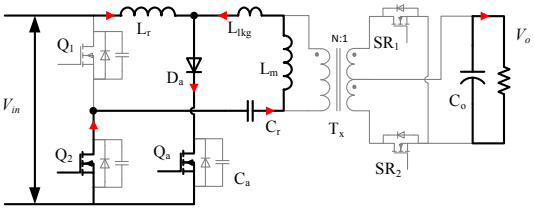

Fig.5 a : mode 1

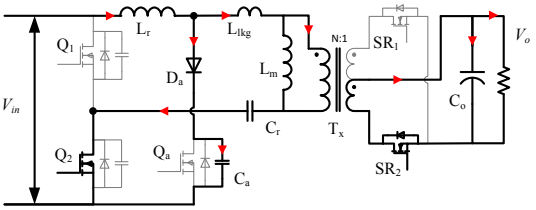

Fig.5 b: mode 2

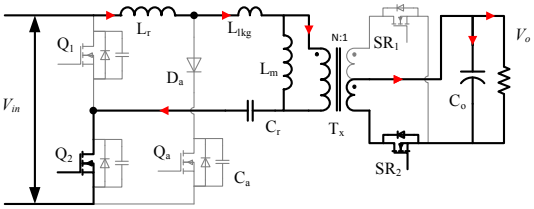

Fig.5 c :mode 3

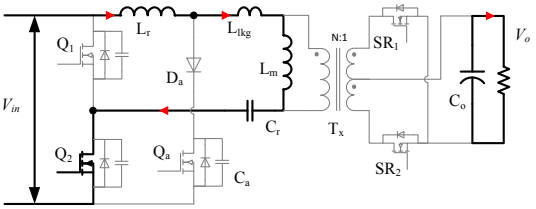

Fig.5 d :mode 4

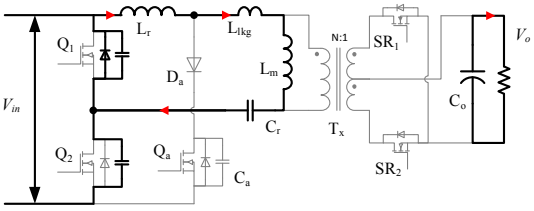

Fig.5 e : mode 5

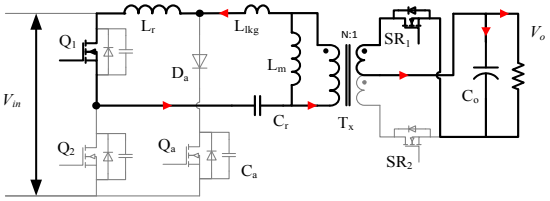

Fig.5 f: mode 6

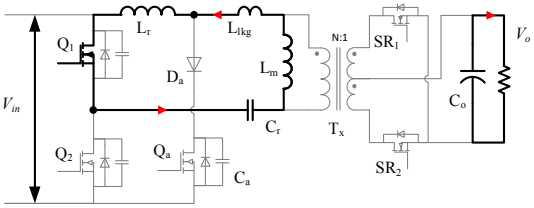

Fig.5 g : mode 7

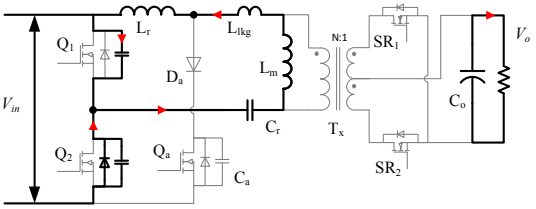

Fig.5 h : mode 8

Fig. 5. Equivalent circuit of the proposed sLLC converter in hold-up state

III. Circuit Analysis Of The Proposed Converter

In this section, key characteristics and design considerations of the proposed sLLC converter during hold up period will be presented. Behaviors of the equivalent circuit in each mode will be analyzed and expressed in fundamental physics and mathematics. LLC converter naturally has no close-form solution of currents and voltages due to the nonlinear characteristics. To relieve the complexity of the design process, the equivalent circuit of sLLC converter in each mode is simplified to obtain the close-form solution in this analysis. The approximations are made based on the assumptions below:

1) Assumption of extreme case behavior

As stated in Section II, the resonant tank absorbs power only in the positive half cycle. It can be inferred that, for given load power, when the duty cycle of the auxiliary switch increases, the resonant inductor current i_{Lr} increases in the positive half cycle, while decreases in the negative half cycle. It is observed that when the duty cycle is beyond certain value, the power transfer in the negative half cycle will reduce to zero. The resonant inductor current i_{Lr} will always be equal to the magnetizing current i_{Lm} during the negative half cycle. The analysis in Section III will be based on the assumption that all load power is transferred during the positive half cycle, as it indicates the extreme operation condition in terms of the voltage gain capacity, and the worst case in terms of component stresses.

Fig. 6 shows the waveforms of simplified sLLC converter in extreme case. In addition to the nomenclature used in Fig. 4, i_{Cr} is the current in the resonant capacitor; I_{Lm_bias} is the DC bias in the magnetizing inductor; D is the duty cycle of the auxiliary switch; T_s is the period of one switching cycle; T_r is the period of a resonant cycle that $T_r = 2\pi\sqrt{L_r C_r}$. To distinguish between the simplified circuit and the actual circuit, the time instant will be τ_0, τ_1… instead of t_0, t_1… used in Fig. 4.

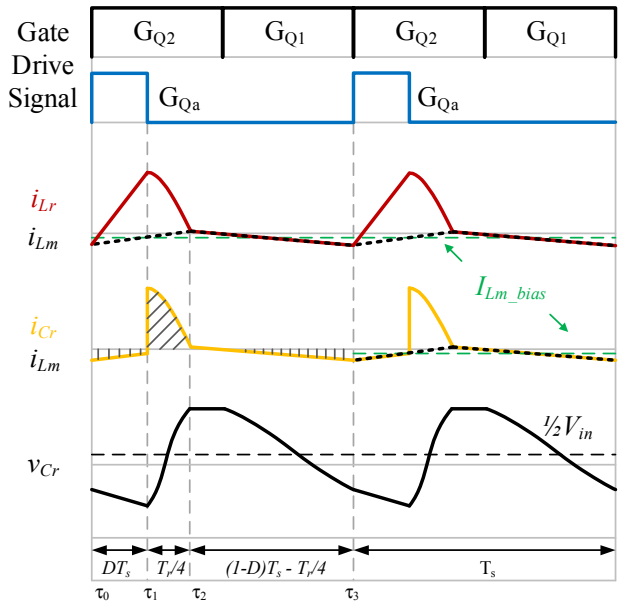

Fig. 6. Key waveforms of simplified sLLC converter in extreme case

2) Assumption of timing

In one switching cycle, timing can be defined by the resonant inductor current. During τ_0 to τ_1, the time interval DT_s, the auxiliary switch Q_a is ON. The resonant inductor current i_{Lr} increases linearly. Instantaneously Q_a turns OFF, i_{Lr} resonates in a sinusoidal shape until it meets i_{Lm}. This period of time (τ_1 to τ_2) is roughly $T_r/4$. It could be understood in the means that i_{Lr} drops from the peak value to 0 in a quarter of one resonant cycle of L_r and C_r. The actual time length may be influenced by the duty cycle D. Generally speaking, when D is very large, the resonant period is slightly below $T_r/4$, and vice versa. In this section, the resonant period is fixed at $T_r/4$. In the rest of the switching cycle (τ_2 to τ_3), no power will be transferred to the load, and i_{Lr} is always equal to i_{Lm}.

3) Assumption of resonant tank currents

In real case, the magnetizing current i_{Lm} is linear only when the power stage transfers power to the load; otherwise i_{Lm} should be sinusoidal. In this approximation, the magnetizing current i_{Lm} will have a triangular shape. More details will be included in the following part.

When the duty cycle of the auxiliary switch D is high, resonant current i_{Lr} is of much higher value than the magnetizing current i_{Lm}, so that i_{Lm} can be neglected in i_{Lr} dominated calculation such as the input charge calculation. Currents in the parasitic components will also be neglected.

4) Assumption of resonant tank parameters

As the parameter design for hold up mode is decoupled with 400V case, it is also assumed that a set of well-designed resonant tank parameters are already obtained to achieve high efficiency for 400V operation. In this section, parameters and specifications in Table I will be used for the analysis.

A. Current stress of switches

During the hold up operation period, the HB bottom switch, the auxiliary switch and diode will have the same peak current as that in the resonant inductor.

The magnetizing current i_{Lm} is very low compared with i_{Lr}. Considering $i_{Lm} = 0$, the initial resonant current i_{Lr} will also be zero. The peak value I_{Lr_pk} can be calculated by (1).

$$I_{Lr\_pk} = \frac{V_{in}}{L_r} \cdot DT_s \tag{1}$$

For the HB top switch, the current is low during hold up process, so that once 400V design if completed, the selected bottom switch will survive for the hold up period.

B. Output-to-input DC Voltage Gain (conversion ratio)

For sLLC converter (also for HB LLC converter), energy exchange between source and resonant tank occurs only in the positive half cycle [12]. In each switching cycle, during Q_2 is ON, the time integral of the resonant inductor current i_{Lr} is equal to the total input charge. The input energy can then be obtained by multiplying the input charge by the input bus voltage. The output energy in one switching cycle is determined by the average output power and the switching frequency. Assuming 100% efficiency, the input energy should be equal to the output energy according to energy conservation law. Considering constant load current, the relation can be expressed in (2):

$$V_{in} \cdot \int_0^{\frac{T_s}{2}} i_{Lr}(t)dt = \frac{V_o \cdot I_o}{f_s} \tag{2}$$

Equation (3) shows the total input charge during the positive half cycle.

$$\int_0^{\frac{T_s}{2}} i_{Lr}(t)dt = \int_0^{DT_s} \frac{I_{Lr\_pk}}{DT_s} \cdot tdt + \int_{\frac{T_r}{4}}^{\frac{T_r}{2}} I_{Lr\_pk} \sin(\frac{2\pi}{T_r}t)dt \tag{3}$$

Combining (1), (2), and (3), the analytical expression of the output voltage V_o can be found in (4):

$$V_o = \frac{V_{in}^2 D}{L_r I_o}\left(\frac{D}{2f_s} + \sqrt{L_r C_r}\right) \tag{4}$$

It could be seen that the output voltage will increase monotonically with duty cycle D increases.

C. Magnetizing current with DC bias

The asymmetrical current waveform between positive half cycle and negative half cycle will introduce a DC bias I_{Lm_bias} on the magnetizing inductor current. In steady state, ampere-second balance must be achieved on the resonant capacitor. If

the average value is i_{Lm} is 0 during τ_1 to τ_2, I_{Lm_bias} can be found in (5):

$$I_{Lm\_bias} = \frac{1}{T_s}\int_{\frac{T_r}{4}}^{\frac{T_r}{2}} I_{Lr\_pk}\sin(\frac{2\pi}{T_r}t)dt = I_{Lr\_pk} f_s \sqrt{L_r C_r} \quad (5)$$

In real case, the magnetizing current reach the maximum value I_{Lm_max} at time instant τ_2, and the minimum value I_{Lm_min} occurs near the time instant τ_1. The magnetizing inductor current is sinusoidal and near symmetrical during time interval τ_1 to τ_2 and τ_2 to τ_3. Thus it is reasonable to assume the slope of the linearized magnetizing current be of the same absolute value. Assuming the slope is k, there is:

$$\Delta I_{Lm} = I_{Lm\_\max} - I_{Lm\_\min} = kDT_s + \frac{nVo}{L_m}\frac{T_r}{4} = k\left[(1-D)T_s - \frac{T_r}{4}\right] \quad (6)$$

Then the peak value of the magnetizing current can be obtained by (7):

$$I_{Lm\_pk} = I_{Lm\_\min} = I_{Lm\_bias} - \frac{\Delta I_{Lm}}{2} = I_{Lr\_pk}\sqrt{L_r C_r} f_s - \frac{nV_o}{L_m}\left(\frac{\pi\sqrt{L_r C_r}D}{2(1-2D)-\pi\sqrt{L_r C_r} f_s} + \frac{\pi\sqrt{L_r C_r}}{2}\right) \quad (7)$$

D. Resonant capacitor voltage stress

During the positive half cycle, the positive portion of the resonant inductor current i_{Cr} (i.e. i_{Lr}) will charge the resonant capacitor C_r from the minimum value V_{Cr_min} to the maximum value V_{Cr_max}. Neglecting i_{Lm}, V_{Cr_min} occurs near the time instant τ_1, then i_{Lr} will charge C_r to V_{Cr_max} at around time instant τ_2. This can be expressed by (8):

$$\Delta V_{Cr} = V_{Cr\_\max} - V_{Cr\_\min} = \frac{1}{C_r}\int_{\frac{T_r}{4}}^{\frac{T_r}{2}} I_{Lr\_pk}\sin(\frac{2\pi}{T_r}t)dt = I_{Lr\_pk}\sqrt{\frac{L_r}{C_r}} \quad (8)$$

Considering the $V_{in}/2$ bias on C_r, the peak voltage stress on the resonant capacitor is given in (9):

$$V_{Cr\_pk} = V_{Cr\_\max} = \frac{V_{in}}{2} + \Delta V_{Cr} = \frac{V_{in}}{2} + I_{Lr\_pk}\sqrt{\frac{L_r}{C_r}} \quad (9)$$

IV. Experiment Results

A 250V-400V input, 12V/300W output prototype was built to verify effectiveness the proposed sLLC converter and its hold up ability. The detailed design requirement and power train parameters are given in Table 1.

TABLE I. Specifications of sLLC Converter

Input voltage	250V-400V
Output voltage/power	12V/300W
Transformer turns ratio	17:1
Resonant inductor	24μH
Resonant Capacitor	12nF
Magnetizing inductor	250μH
Leakage inductor	6μH
Output capacitor	2mF
HB MOSFETs	IPW60R190C6
SR MOSFETs	SiRA00DP
Auxiliary MOSFET	C2M0160120D
Auxiliary Diode	APT60D60BG
Auxiliary capacitor	2nF

Fig. 7 shows the steady state waveforms of sLLC converter under 300W full load operating at 400V input voltage. The switching frequency is 240 kHz. It is lower than the designed resonant frequency due to the impact of the leakage inductor of the transformer. The resonant current is close to sinusoidal. The peak value is 3A.

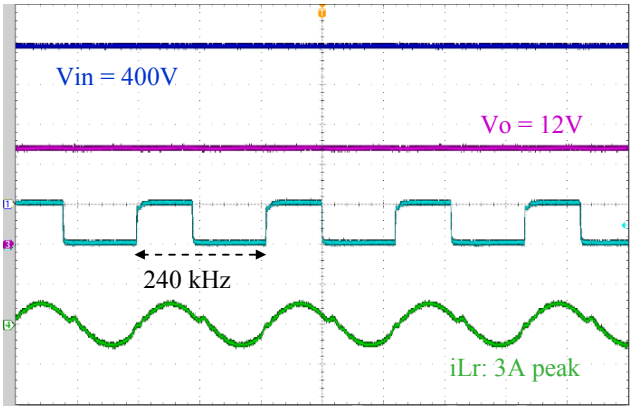

Fig. 7. 400V input, 12V/25A full load steady state waveform

Fig. 8 shows the steady state waveforms of sLLC converter under 300W full load operating at 250V input voltage. HB switches are operating at the minimum frequency at 140kHz. The duty cycle of the auxiliary switch is around 0.12. The peak value of the inductor current is 8A.

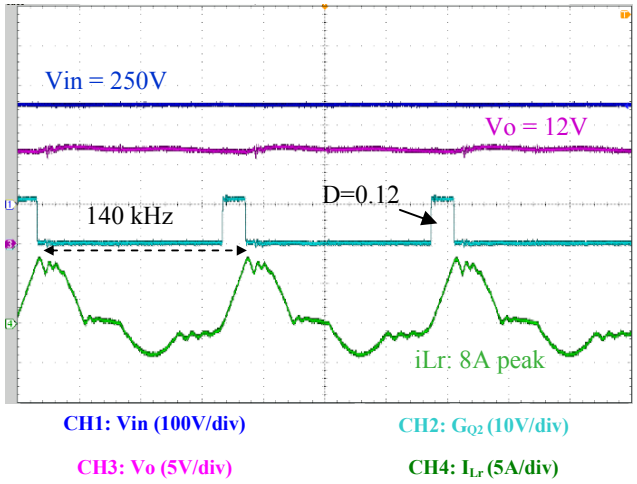

Fig. 8. 250V input, 12V/25A full load steady state waveform

Fig. 9 shows the hold-up process under full load. When the input voltage is between 400V and 320V, the auxiliary switch is OFF, and frequency modulation of HB switches regulates the output voltage. When the input voltage drops below 320V, Q_a starts to take over the output voltage regulation. It could be observed that the output voltage does not lose regulation until the input voltage drops below 250V.

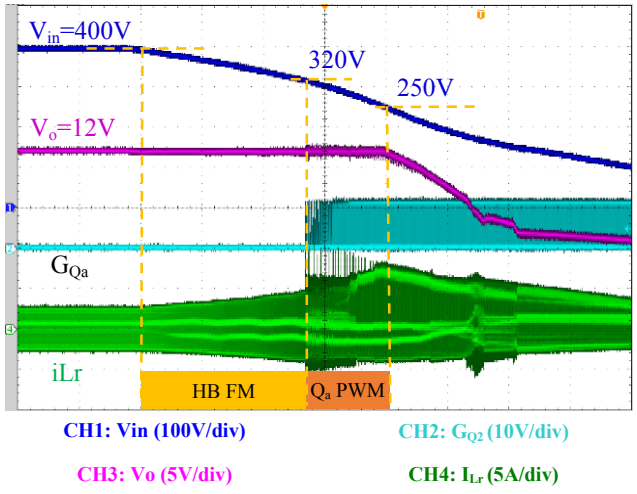

Fig. 9. 12V/25A full load dynamic waveform

Fig. 10 shows the steady state waveforms of sLLC converter under 12V/15A 60% load operating at 400V input voltage. The switching frequency is 250 kHz. The resonant current is close to sinusoidal. The peak value is 1.8A.

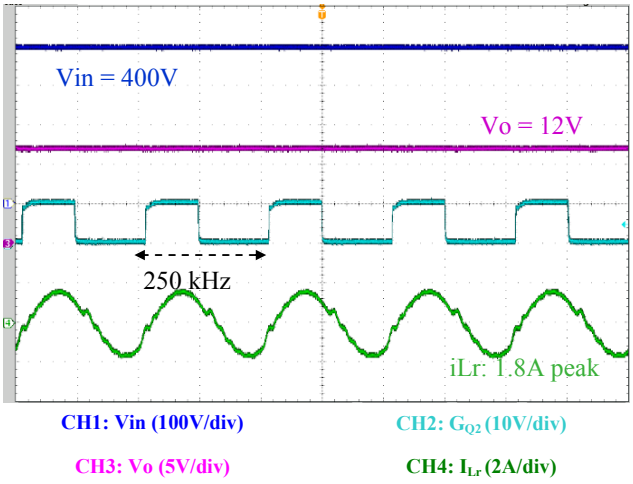

Fig. 10. 400V input, 12V/15A 60%load steady state waveform

Fig. 11 shows the steady state waveforms of sLLC converter under 12V/15A 60% load operating at 250V input voltage. HB switches are operating at the minimum frequency at 140kHz. The duty cycle of the auxiliary switch is around 0.09. The peak value of the inductor current is 5A.

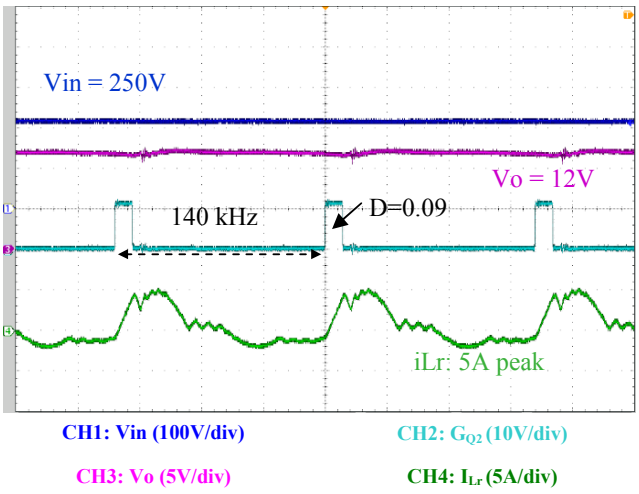

Fig. 11. 250V input, 12V/15A 60%load steady state waveform

Fig. 12 shows the hold-up process under 15A (60% load). Output voltage can be regulated by frequency modulation of HB switches till 300V input. Between 300V and 210V, Q_a operates in PWM mode to hold the output voltage at 12V.

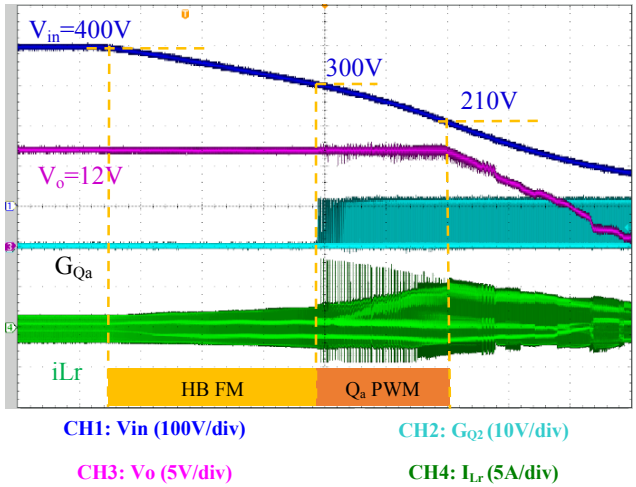

Fig. 12. 12V/15A 60% load dynamic waveform

V. Conclusion And Future Work

In this paper, a new HB LLC converter with auxiliary switch (sLLC) is proposed to solve the hold-up problems in server and telecommunication power applications. The proposed sLLC converter is suitable for low voltage application where SR is needed. The magnetizing inductor L_m can be integrated into the transformer core to reduce the converter size. Also, L_m can be designed with large value to reduce the circulation loss. During 400V input, the auxiliary switch will not conduct and the circuit operation is same as the conventional LLC converter. When input voltage is low, the auxiliary switch is turned on to increase the resonant inductor energy in one switching cycle, thus hold up operation is achieved that the output voltage can be maintained at 12V. A 250V-400V input, 300W prototype has been built to verify the feasibility and effectiveness of the proposed sLLC converter.

References

[1] B. Yang and F. C. Lee, "LLC Resonant Converter for Front End DC / DC Conversion," in Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE, 2002, vol. 2, pp. 1108–1112.

[2] Y. Chen, H. Wang, Z. Hu, Y.-F. Liu, J. Afsharian, and Z. A. Yang, "LCLC resonant converter for hold up mode operation," in Energy Conversion Congress and Exposition (ECCE), 2015 IEEE , vol., no., pp.556-562, 20-24 Sept. 2015

[3] H. Wang, Y. Chen, Y.-F. Liu, J. Afsharian, and Z. A. Yang, "A new LLC converter family with synchronous rectifier to increase voltage gain for hold-up application," in Energy Conversion Congress and Exposition (ECCE), 2015 IEEE , vol., no., pp.5447-5453, 20-24 Sept. 2015

[4] Y. Xing, L. Huang, X. Cai, and S. Sun, "A Combined Front End DC / DC Converter," in Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE, 2003, vol. 00, no. C, pp. 1095–1099.

[5] B. Yang, P. Xu, and F. C. Lee, "Range winding for wide input range front end DC/DC converter," APEC 2001. Sixth. Annual. IEEE Appl. Power Electron. Conf. Expo. (Cat. No.01CH37181), vol. 1, pp. 476–479, 2001.

[6] M.-Y. Kim, B.-C. Kim, K.-B. Park, and G.-W. Moon, "LLC series resonant converter with auxiliary hold-up time compensation circuit," 8th Int. Conf. Power Electron. - ECCE Asia, pp. 628–633, May 2011.

[7] B.-C. Kim, K.-B. Park, and G.-W. Moon, "LLC resonant converter with asymmetric PWM for hold-up time," in Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on, 2011, pp. 38 – 43.

[8] B.-C. Kim, K.-B Park, S.-W. Choi, and G.-W. Moon, "LLC series resonant converter with auxiliary circuit for hold-up time," INTELEC 2009 - 31st International Telecommunications Energy Conference, 1–4. doi:10.1109/INTLEC.2009.5351749

[9] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A Half-Bridge LLC Resonant Converter Adopting Boost PWM Control Scheme for Hold-Up State Operation," IEEE Trans. Power Electron., vol. 29, no. 2, pp. 841–850, Feb. 2014.

[10] J. Kim and G. Moon, "A New LLC Series Resonant Converter with a Narrow Switching Frequency Variation and Reduced Conduction Losses," IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4278–4287, 2014.

[11] H. Wu, T. Mu, X. Gao, and Y. Xing, "A Secondary-Side Phase-Shift-Controlled LLC Resonant Converter With Reduced Conduction Loss at Normal Operation for Hold-Up Time Compensation," Application. Power Electronics, IEEE Transactions on, 30(10), 5352 − 5357. doi:10.1109/TPEL.2015.2418786

[12] Z. Hu; Y.-F. Liu; P.C. Sen, "Cycle-by-cycle average input current sensing method for LLC resonant topologies," Energy Conversion Congress and Exposition (ECCE), 2013 IEEE , vol., no., pp.167,174, 15-19 Sept. 2013